



CLAS12 Solenoid Pre-Power-Up Interlock Checkout

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Description

- The pre-power-up interlock checkout is the procedure performed prior to full current magnet operation to verify I&C interlocks are operational
 - Originally comprised of 31 tasks, some of which have multiple sub-tasks
 - B00000400-P005 in document control

Common Steps

- Most of the tasks require all interlocks to be cleared
- Then a fault is raised, either physically or via software
 - Check that proper response is initiated
 - Some faults are reported on Sequence Of Events (SOE) module which has corresponding LED relays
- Clear faults

Lead Water Flow

- Task 2 (Supply) & 3 (Return)
 - Both cause fast dump + displayed on SOE
 - Opposite flow slow switch is jumpered out to prevent fault, water is valved off causing fault on tested lead

Cables

- Task 4 (Voltage Taps) & 5 (System)
 - Both cause fast dump + displayed on SOE
- Procedure for 4 was modified to use connectors on panel instead of feed-throughs on SST and magnet
 - Reduced number of dumps from 10 to 4
- Procedure for 5 was modified to disconnect only the interlock wire from terminal block instead of the sensor cables on feed-throughs
 - This prevented any sensors from being lost

Helium Reservoirs

- Liquid Level
 - Task 6 (Magnet) & 7 (Leads)
 - Both cause fast dump + displayed on SOE
 - Low level setpoint is set below current level on hardware unit to cause the fault, so requires helium to be present
 - Per Ruben, Task 7 was modified to not cause fast dump or clear interlocks (only displayed on SOE) due to checking for lead short
 - Task 26 (Leads) & 27/28 (Magnet, 2 sensors)
 - Cause controlled ramp
 - Set threshold above current liquid level on PLC to cause fault
- Pressure
 - Task 24 (Lead) & 25 (Magnet)
 - Cause a controlled ramp
 - Lower threshold to cause a fault

Quench Detection

- Task 8 (QD 1) & 9 (QD 2)
 - Both cause fast dump + displayed on SOE
 - Done by Probir during QD retuning
- Task 14 (2nd) & 21 (1st) PLC QD Calculation
 - Place voltage source on test panel, increase until interlock is tripped
 - 2nd causes fast dump + displayed on SOE
 - 10 comparators
 - 2 were too noisy to test
 - 1st is controlled ramp
 - 6 comparators

Load Cells

- Task 17 (1st) & 32 (2nd)
 - Done for all 16 load cells
 - Threshold is set lower than current sensor value
 - 1st causes controlled ramp
 - 2nd causes fast dump + displayed on SOE
 - Was initially missing from procedure

Temperatures

- Task 10 (Splice) & 11 (Leads)
 - Both cause fast dump + displayed on SOE
 - Cryocon setpoints are changed such that relay is turned off causing fault
- Task 18 (VCL) & 19 (WCL)
 - Both cause controlled ramp
 - Temporary tag assigned to comparison to cause fault

Voltages

- Task 15 Vapor Cooled Leads
 - VT1 & VT19
 - Causes fast dump + displayed on SOE
 - Assigned temporary tag with value greater than comparison limit causes fault

Misc Interlocks

- Task 12 is Fast Dump button on EPICS screen
 - Simply push button to cause dump
 - Need to confirm before dump happens
- A temporary tag is assigned to comparison, which has value higher/lower than limit which causes fault
 - Fast Dumps
 - Task 13 is hard coded limit on PLC
 - Task 16 is UPS battery low
 - Controlled Ramp Down
 - Task 20 Fast DAQ cRIO Communications
 - Task 22 Vacuum
- Task 29 Software current limits
 - Verify that current can't be entered above limit on EPICS screen
- Task 31 Controlled Ramp Down Warning
 - Simulates ramp down failure

Misc Interlocks 2

- Task 1 PLC Watchdog
 - Fast dump + displayed on SOE
 - Remove timer relay used to indicate PLC is operational

Skipped Tasks

- Task 23 EPICS watchdog
 - EPICS heartbeat does not get set to PLC
- Task 30 End Station Refrigerator (ESR)
 - The wired connection is allocated but not connected on PLC

Conclusion

- Procedure completed
 - <https://logbooks.jlab.org/entry/3484233>
- Revision with changes to procedure in progress
- Magnet ready for full current power-up